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Attorney Docket No.:FUJS 14.330A

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Inventor: Yoshinori NAKAMURA et al.

Serial No.:

Filed: November 16, 2001

Title: **FRAME SYNCHRONOUS PATTERN PROCESSING APPARATUS AND FRAME SYNCHRONOUS PATTERN DETECTION APPARATUS AND METHOD FOR DETECTING FRAME SYNCHRONOUS PATTERN**

Examiner:

Group Art Unit:

Assistant Commissioner for Patents
Washington, D.C. 20231

PRELIMINARY AMENDMENT

SIR:

Prior to examination on the merits and prior to calculating the filing fee, please amend the above-captioned application as follows:

IN THE SPECIFICATION

On page 1, line 5, please insert the following:

--CROSS REFERENCE TO RELATED APPLICATION

This is a continuation of Application No. 08/880,723, filed on June 23, 1997.--

IN THE CLAIMS

Please cancel claims 1-17, without prejudice or disclaimer.

Please rewrite claims 18 to 20 as follows:

18. (Once Amended) A frame synchronous pattern detection apparatus, for detecting an actual frame synchronous pattern which is a part of a frame synchronous pattern and is essential to execute frame synchronizing, comprising:

(a) a provisional-region detection section; and

(b) a frame synchronous pattern detecting section,

said provisional-region detection section being for sampling, from parallel data according to a synchronous digital hierarchy (SDH) transmission system, a part of the parallel data in which said actual frame synchronous pattern is presumably included, as provisional region data and for outputting the provisional region data in serial form to said frame synchronous pattern detecting section,

said frame synchronous pattern detecting section, communicatively connected with said provisional-region detection section, for detecting said actual frame synchronous pattern from the inputted provisional region data.

19. (Once Amended) A frame synchronous pattern detection apparatus for detecting an actual frame synchronous pattern which is a part of a frame synchronous pattern and is essential to execute frame synchronizing, comprising:

(a) a provisional-region detection section; and

(b) a frame synchronous pattern detecting section,

said provisional-region detection section being for sampling, from given data, a part of parallel data in which said actual frame synchronous pattern is presumably included, as provisional region data, and for outputting the provisional region data in serial form to said frame synchronous pattern detecting section,

said frame synchronous pattern detecting section, communicatively connected with said provisional-region detection section, for detecting said actual frame synchronous pattern from the inputted provisional region data.

20. (Once Amended) A frame synchronous pattern detection method, for detecting an actual frame synchronous pattern which is a part of a frame synchronous pattern and is essential to execute frame synchronizing, said method comprising the steps of:

sampling, from given parallel data, a part in which said actual frame synchronous pattern is presumably included, as provisional region data; and

detecting said actual frame synchronous pattern from said sampled provisional region data converted into serial form.

Please add new claims 21-23 as follows:

--21. A frame synchronous pattern detection apparatus comprising:

(a) a provisional-region detection section for sampling, from parallel data according to a synchronous digital hierarchy (SDH) transmission system, a part of the parallel data in which an object frame synchronous pattern is presumably included, as provisional region data; and

(b) a frame synchronous pattern detecting section for detecting, from said provisional region data, the object frame synchronous pattern,

said provisional region data being output in serial form from said provisional-region detection section to said frame synchronous pattern detecting section.--

--22. A frame synchronous pattern detection apparatus comprising:

(a) a provisional-region detection section for sampling, from given data, a part of parallel data in which an object frame synchronous pattern is presumably included, as provisional region data; and

(b) a frame synchronous pattern detecting section for detecting, from said provisional region data, the object frame synchronous pattern,

said provisional region data being output in serial form from said provisional-region detection section to said frame synchronous pattern detecting section.--

--23. A frame synchronous pattern detection method comprising the steps of:

sampling, from given parallel data, a part in which an object frame synchronous pattern is presumably included, as provisional region data; and

detecting the object frame synchronous pattern using said sampled provisional region data converted into serial form.--

REMARKS

Attached hereto is a marked-up version of the changes made to the claims by the current amendment. The attached pages are captioned "**VERSION WITH MARKINGS TO SHOW CHANGES MADE.**"

Claims 18-23 are pending in the application, claims 21-23 having been added by this amendment, and claims 1-17, having been cancelled, without prejudice or disclaimer, since they are pending in parent application number 08/880,723, filed on June 23, 1997, (hereinafter "the parent application").

Claims 18-23 were rejected under 35 U.S.C. §102(b) in the Office Action mailed in the parent application on July 16, 2001, (hereinafter "the Office Action"), as being anticipated by new over Suh et al., (U.S. Patent No. 5,710,774).

Claims 20 and 23 were rejected under 35 U.S.C. §102(b) in the Office Action as being anticipated over Obana et al., (U.S. Patent No. 5,136,587).

Claims 18 and 19, dealing with a frame synchronous pattern apparatus, recite that the apparatus is for detecting an actual frame synchronous pattern, which is a part of a frame synchronous pattern and is essential to execute frame synchronizing, and comprises (a) a provisional-region detection section, and (b) a frame synchronous pattern detecting section, the provisional-region detection section sampling from parallel data a part of the parallel data in which an actual frame synchronous pattern is presumably included as provisional region data and outputting the provisional region data in serial form to the frame synchronous pattern detecting section.

Claim 20, dealing with a frame synchronous pattern detection method, provides for sampling, from given parallel data, a part in which the actual frame synchronous

pattern is presumably included, as provisional region data, and detecting the actual frame synchronous pattern from the sampled provisional region data converted into serial form.

The feature of the actual frame synchronous pattern in claims 18-20, is supported by the specification on page 40, lines 8-26, and by Fig. 4 of the drawings. The feature of converting and outputting the provisional-region data in serial form is supported in the specification by, for example, page 23, line 26, to page 24, line 3.

Consequently, a hypothetical combination of Obana et al. and Suh et al. would not disclose, teach, or suggest the subject matter of amended claims 18-20 since such a hypothetical combination lacks the Applicants' concept of detecting an actual frame synchronous pattern, which is a part of a frame synchronous pattern, and is essential to execute frame synchronizing.

The Examiner states that Suh et al. discloses a first comparison circuit 40, a second comparison circuit 50, and a selection circuit 60 which he equates to the provisional-region detection section claimed in claims 18-19, (Office Action, page 4, line 21 to page 5, line 1). In addition, the Examiner finds that the synchronizing pattern detecting circuit 90 in Suh et al. is the equivalent of the frame synchronous pattern detecting section claimed in claims 18-19, (Office Action, page 5, lines 5-10).

Claims 18 and 19 indicate that the provisional- region data is output from the provisional-region detection section to the frame synchronous pattern detection section. In contrast, in Suh et al., the synchronizing pattern detecting circuit 90 does not receive provisional-region data in serial form which is part of the parallel data in which an object frame synchronous pattern is presumably included. Rather, the synchronizing pattern detecting circuit 90 receives one of the two signals X1, or X2, which are output from the

selecting circuit 60, and a signal derived from the reference clock, (Suh et al., column 3, line 54 - column 4, line 18; column 5, lines 23-32; Figs. 1, 2B).

The Examiner attempts to equate the output signals X1 or X2 to the provisional-region data claimed in claims 18-23 by reasoning which, it is respectfully submitted, is incorrect. The Examiner states that the output signals result from the comparison of the input parallel data to the A1 bytes at the first comparison circuit (40) and to the A2 bytes at the second comparison circuit (50). Based upon this statemsent, he concludes that the output signals are a part of the parallel data input from the serial/parallel converter 10, (Office Action, page 4, lines 1-5). This conclusion is flatly contradicted by Fig. 1 of Suh et al. which shows X1 and X2 as being output from the first and second comparison circuits 40, 50 and not as part of the parallel data inputted from the serial/parallel converter 10 to the comparison circuits 40, 50. X1 and X2 are not fed back as part of the parallel data inputted from the serial/parallel converter 10. Furthermore, X1 and X2 cannot be equated in this way to the provisional-region data, which is claimed to be in serial form, when the data inputted from the serial/parallel converter 10 is in parallel form.

With regard to Obana et al., the Examiner indicates that a detection circuit 61 detects frame synchronizing patterns from a multiplexed signal, (Office Action, page 4, lines 2-5). However, according to Obana et al., the detection circuit 61 detects frame synchronizing patterns A1 and A2 from an input serial signal, (column 8, line 41 - column 9, line 2; Fig. 8). It is clear, however, from claim 20, in contrast, that the sampling step claimed in that claim uses given parallel data. Furthermore, the sampling step claimed in claim 20 is nowhere disclosed, taught, or suggested in Obana et al. With

regard to Suh et al., claim 20 specifies that the sampled provisional-region data is converted to serial form and, as argued previously, the data inputted from the serial/parallel converter 10 is in parallel form. Moreover, X1 and X2 in Suh et al. are nowhere disclosed to be serial data converted from parallel sampled provisional-region data, as claimed in claim 20.

New claims 21-23 have been added to afford the Applicants additional claim coverage. Claims 21-22 indicate that the provisional-region data is output in serial form from the provisional-region detection section to the frame synchronous pattern detecting section analogously to claims 18-19, and therefore, are patentably distinguishable over Suh et al., for the same reasons given above with respect to those features in claims 18 and 19. In addition, claim 23, analogously to claim 20, indicates that the sampling step uses given parallel data, and that the detecting step uses data converted to serial data, and therefore, this claim is patentably distinguishable over Obana et al., and Suh et al., for the same reasons given above with respect to claim 20.

Finally, claim 23 indicates that the frame synchronous pattern detection method comprises a step of detecting the object frame synchronous pattern using said sampled provisional region data. This feature of claim 23 patentably distinguishes over Suh et al. since, according to the analysis of the Examiner, Suh et al. does not use the sampled provisional region data to detect the object frame synchronous pattern, but merely uses one of the two comparison signals X1 or X2, (column 3, line 65 - column 4, line 1; column 5, lines 23-32; Figs. 1, 2B).

CLOSING

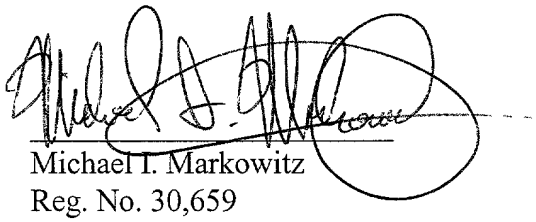
An earnest effort has been made to be fully responsive to the Examiner's objections. In view of the above amendments and remarks, it is believed that independent claims 18-23 are in condition for allowance as well as those claims dependent therefrom. Passage of this case to allowance is earnestly solicited.

It is respectfully requested that this amendment be entered prior to calculation of the filing fee so that Applicants are not charged for the pendency of claims 1 to 17 prior to entry of this amendment.

However, if for any reason the Examiner should consider this application not to be in condition for allowance, he is respectfully requested to telephone the undersigned attorney at the number listed below prior to issuing a further Action.

Any fee due with this paper, not fully covered by an enclosed check, may be charged on Deposit Account 50-1290.

Respectfully submitted,



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Enclosure: Version with Markings to Show Changes Made

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

IN THE CLAIMS

Claims 18 to 20 have been rewritten as follows:

18. (Once Amended) A frame synchronous pattern detection [apparatus] apparatus, for detecting an actual frame synchronous pattern which is a part of a frame synchronous pattern and is essential to execute frame synchronizing, comprising:

[a temporary region detection section for temporarily detecting a candidate of region data which may contain a frame synchronous pattern from multplex data including said frame synchronous pattern based on a SDH transmission system; and]

(a) a provisional-region detection section; and

(b) a frame synchronous pattern detecting section,

said provisional-region detection section being for sampling, from parallel data according to a synchronous digital hierarchy (SDH) transmission system, a part of the parallel data in which said actual frame synchronous pattern is presumably included, as provisional region data, and for outputting the provisional region data in serial form to said frame synchronous pattern detecting section,

[a frame synchronous pattern detection section for detecting said frame synchronous pattern from said temporary region data detected in said temporary region detection section.]

said frame synchronous pattern detecting section, communicatively connected with said provisional-region detection section, for detecting said actual frame synchronous pattern from the inputted provisional region data.

19. (Once Amended) A frame synchronous pattern detection [apparatus] apparatus, for detecting an actual frame synchronous pattern which is a part of a frame synchronous pattern and is essential to execute frame synchronizing, comprising:

[a temporary region detection section for temporarily detecting a candidate of region data which may contain a given frame synchronous pattern from data including said frame synchronous pattern; and]

(a) a provisional-region detection section; and

(b) a frame synchronous pattern detecting section,

said provisional-region detection section being for sampling, from given data, a part of parallel data in which said actual frame synchronous pattern is presumably included, as provisional region data, and for outputting the provisional region data in serial form to said frame synchronous pattern detecting section,

[a frame synchronous pattern detection section for detecting said frame synchronous pattern from said temporary region data detected in said temporary region detection section.]

said frame synchronous pattern detecting section, communicatively connected with said provisional-region detection section, for detecting said actual frame synchronous pattern from the inputted provisional region data.

20. (Once Amended) A frame synchronous pattern detection [method apparatus for] method, for detecting an actual frame synchronous pattern which is a part of a frame synchronous pattern and is essential to execute frame synchronizing, said method comprising the steps of: [temporarily detecting a candidate of region data which may

contain a given frame synchronous pattern from data including said frame synchronous pattern, and for detecting said frame synchronous pattern from said temporary region data.]

sampling, from given parallel data, a part in which said actual frame synchronous pattern is presumably included, as provisional region data; and

detecting said actual frame synchronous pattern from said sampled provisional region data converted into serial form.